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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,913	10/03/2000	Gary S. Ditlow	BUR9-2000-0024-US1	4668

7590 04/22/2004

ATTEN: GEORGE R. PETIT
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EXAMINER	
BRODA, SAMUEL	
ART UNIT	**PAPER NUMBER**
2123	4

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,913	DITLOW ET AL.	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2. ✓
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Information Disclosure Statement

2. The Information Disclosure Statement by Applicant ("IDS"), Paper No. 2, listed Farbarik et al, "CAD Tools for Area Distributed I/O Pad Packaging," but only a copy of its Abstract appeared in the publications submitted with the IDS. A copy of this publication was located by the Examiner and the citation is listed on the Form PTO-892 "Notice of References Cited" included with this Office Action.

Drawings

3. The Draftsperson has objected to the drawings; see the copy of Form PTO-948 for an explanation.

Claim Rejections - 35 U.S.C. § 112, First Paragraph

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.1 Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

4.2 Regarding dependent claim 8, this claim is directed at a limitation for "adjusting a granularity of said resistance model for a desired accuracy of said model."

The broadest reasonable interpretation of this limitation suggests a known correlation between the granularity of the resistance model and the accuracy of the results, so that the user could adjust the granularity to reach a desired accuracy. However, the only description of the granularity appears in the Specification at page 6, lines 17-23, stating:

> Moreover, the resistance model may be expressed in different degrees of granularity. Typically, different levels of granularity would yield different X-Y locations for nodes of [the] resistance model. For example, in a model of fine granularity, each I/O circuit would be closer to at least one node of the resistance model than would be the case, for the average I/O circuit, in a resistance model of coarse granularity. The degree of granularity utilized would depend on the accuracy of the model needed in order to achieve acceptable results as determined by a user.

While this description appears to suggest a correspondence between the granularity and the accuracy, it does not describe the type of correlation permitting the user to achieve a "desired accuracy" by adjusting the granularity.

Claim Rejections - 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the date of invention thereof by the applicant for patent.

5.1 Claims 1-4, 7, 9, and 11-15 are rejected under 35 U.S.C. 102(a) as being anticipated by Buffet et al, "Methodology for I/O Cell Placement and Checking in ASIC Designs Using Area-Array Power Grid," Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, pp. 125-128 (May 2000).

5.2 Regarding claim 1, Buffet et al teaches a method and system for performing power distribution analysis for I/O circuits in an integrated circuit (IC) design, the I/O circuits having defined placement locations within a power distribution network of said design, comprising the steps of:

a) calculating maximum and average currents for each of said I/O circuits, and an average logic current demand per node [maximum, average and bump currents calculated as part of electrical checking programs; see page 128 Section "Electrical Checking of Every Design"];

b) creating a resistance model of said power distribution network comprising nodes and resistors corresponding to points on buses of said network and resistivities corresponding to said points [resistance model calculated as part of windowing process; see page 127 Section "Rule Generation"];

c) indexing each of said I/O circuit currents and said average logic current demand per node to the node in said model closest to the corresponding 1/O circuit location [windowing of power grid corresponds to indexing; see pages 126-127 Section "Power-Grid Modelling and Analysis" and Fig. 4];

d) solving the resistance and current source model resulting from step (c) for voltages at the nodes [resistance and current source models (equations (1)-(4)) used to solve for voltages windows, power buses, and bumps]; and

e) outputting the results [results output as indicated at page 127 column 2 paragraph 5 stating "Simulation results establish that the power-grid structure supporting high-current I/O cells can achieve the logic circuit density goals while remaining within the allowable IR and EM limits"].

Therefore, Buffet et al anticipates claim 1.

5.3 Regarding claims 2-3, the method and system of Buffet et al teaches the changing of I/O cell placement to avoid "single cell hot spots" corresponding to EM and IR violations. See page 127 column 1 paragraph 1 and column 2 paragraphs 5-6.

5.4 Regarding claims 7 and 13-15, these independent claims are anticipated using the analysis of claim 1 above.

5.5 Regarding claim 9, the model of Buffet et al uses a lumped effective resistance. See equation (1) page 127.

5.6 Regarding claim 11, the design rules in Buffet et al check for voltage variations corresponding to 'IR drop.' See page 125 column 2 paragraph 1.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.1 Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buffet et al.

6.2 Regarding claim 5, the method and system of Buffet et al does not appear to teach a method of performing a power distribution analysis for a peripheral type I/O circuit distribution, but instead teaches the method as applied to an area-array I/O circuit distribution.

However, the Abstract of Buffet et al supplies the motivation that would instruct one of ordinary skill in the art to apply the method to a peripheral type I/O circuit distribution. The Abstract states:

> Electrical rule checking is fundamental to achieve a good I/O cell placement. This paper presents the analysis techniques used to design a robust power-grid structure, the method used to make I/O cell placement guidelines, details of the I/O cell placement process and electrical checking algorithms.

Regarding claim 5, it would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method and system of Buffet et al to perform power distribution analysis for a peripheral type I/O distribution, because such analysis would be fundamental to achieving good I/O cell placement.

6.3 Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buffet et al, in view of common knowledge regarding circuit analysis.

6.4 Regarding claims 6 and 10, the method and system of Buffet et al does not appear to teach: (1) the use of a sparse matrix solver, and (2) the calculation of voltages based on a combination of current and conductance matrices. Official Notice is taken that both the use of

sparse matrix solvers and the use of voltage calculations based on a combination of current and conductance matrices are old and well known in circuit analysis. The physical structure of circuits often leads to models forming sparse matrices, and similarly circuit voltages follow natural laws involving resistance, conductance, and current.

It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to incorporate: (1) matrix calculations involving current and conductance, and (2) sparse matrix techniques, into the method and system of Buffet et al, because such matrices and matrix calculations would more accurately model physical circuit behavior and provide results corresponding to theoretical calculations.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure. Reference to Rao et al, U.S. Patent 6,225,143, is cited as teaching a tile-based routing between a bump pad and an input/output pad device for implementation on a flip-chip integrated circuit die.

Reference to Hayashi et al, "EMI-Noise Analysis Under ASIC Design Environment," ACM Proceedings of the 1999 International Symposium on Physical Design, pp. 16-21 (September 1999), is cited as teaching a core network power model formed by a grid. See Section 2.1 et seq.

Reference to Kar et al, "Optimizing C4 Bump Placements for a Peripheral I/O Design," 1999 IEEE Proceedings of the 49th Conference on Electric Components and Technology, pp. 250-254 (June 1999), is cited as teaching I/O bump placement for a peripheral I/O design.

Reference to Caldwell et al, "Implications of Area-Array I/O for Row-Based Placement Methodology," 1998 IEEE Symposium on IC/Package Design Integration, pp. 93-98 (February 1998), is cited as teaching a comparison of I/O placement methodologies.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (703) 305-1026. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER